Notice of Allowability	Application No.	Applicant(s)	
	10/025,165	CERVANTES, JOSE L.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *reconsideration filed on 11/21/05*.

2. ☒ The allowed claim(s) is/are *1-24,28,30 and 31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH **PERIOD IS NOT EXTENDABLE**.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

THOMAS LEE
SUPERVISORY PATENT EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven E. Dicke (Reg. No. 38,431) on 12/12/05.

2. The application has been amended as follows:

In the Claims:

Claims 1, 9, 10, 11, 16, 17, 21, 22, 23, 28, 29 and 30 are amended as follows:

1. ([Previously Presented] Currently Amended) A portable computer having a first power mode and a second power mode, comprising:

a first memory bus;

a second memory bus; [and]

a control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode[.]; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first clock speed and the second clock speed.

9. ([Origin] Currently Amended) The computer of claim 8, wherein the first memory bus and the second memory bus are [is] in communication with the chipset.

10. ([Origin] Currently Amended) The computer of claim 1, further comprising an override switch coupled to the control system for switching the first memory bus and the second memory bus to the first speed or the second speed.

11. ([Previously Presented] Currently Amended) A computer having a first battery power mode and a second external power mode, the computer comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; [and]

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus and the second memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode[.]; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first clock speed and the second clock speed.

16. ([Origin] Currently Amended) The computer of claim 8, wherein the first memory bus and the second memory bus are [is] in communication with the chipset, and the chipset is in communication with the clock generator.

17. ([Previously Presented] Currently Amended) A mobile computing device having a first battery power mode and a second external power mode, the device comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; [and]

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus and the second memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode[.]; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first clock speed and the second clock speed.

21. ([Previously Presented] Currently Amended) A method of managing power in a mobile computing device comprising:

determining whether the mobile computing device is operating in a first power mode or a second power mode;

operating a first memory bus and a second memory bus at a first bus speed when the mobile computing device is in the first power mode; [and]

operating the first memory bus and the second memory bus at a second bus speed different from the first bus speed when the mobile computing device is in the second power mode[.]; and

a performance level input for defining the first bus speed and the second bus speed wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first bus speed and the second bus speed.

22. ([Original] Currently Amended) The method of claim 21, further comprising controlling a clock generator to determine the first bus speed and the second bus speed.

23. ([Original] Currently Amended) The method of claim 21, further comprising:

determining the first [memory] bus speed and the second bus speed independent of an internal processor bus speed.

28. ([Previously Presented] Currently Amended) A mobile computing device having a first battery power mode and a second external power mode, the device comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; [and]

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory;

a clock generator in communication with the control system, wherein the control system is configured to operate the first memory bus and the second memory bus at a first clock speed in the first battery power mode, and a second clock speed in the second power mode; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed[.] wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first bus speed and the second bus speed.

29. Cancelled.

30. ([Previously Presented] Currently Amended) The device of claim [29]28, further comprising:

wherein the performance level input is configured to allow a user to select a user defined memory bus speed for the first clock speed and the second clock speed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
December 13, 2005

THOMAS LEE
SUPERVISORY